WEST

Freeform Search

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Term: (image or pictur$4)with (synch$7 or clock$4 or time$4) and (image or picture) near7 (asynch$7) same (combin$7 or synthesi$7 or add$5)same (memory or buffer or register or stor$6) and @ad<19991103

Display: 10 **Documents in Display Format:** - **Starting with Number** 1

Generate: ○ **Hit List** ◉ **Hit Count** ○ **Side by Side** ○ **Image**

Search | Clear | Help | Logout | Interrupt

Main Menu | Show S Numbers | Edit S Numbers | Preferences | Cases

Search History

DATE: Wednesday, June 25, 2003 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,PGPB,JPAB,EPAB,DWPI; PLUR=YES; OP=OR			
L2	(image or pictur$4)with (synch$7 or clock$4 or time$4) and (image or picture) near7 (asynch$7) same (combin$7 or synthesi$7 or add$5)same (memory or buffer or register or stor$6) and @ad<19991103	71	L2
L1	(image or pictur$4)with (synch$7 or clock$4 or time$4) same (image or picture) near7 (asynch$7) same (combin$7 or synthesi$7 or add$5) and @ad<19991103	82	L1

END OF SEARCH HISTORY

L2: Entry 17 of 71 File: USPT Nov 28, 2000

B

DOCUMENT-IDENTIFIER: US 6154202 A
TITLE: Image output apparatus and image decoder

Abstract Text (1):
An image output apparatus capable of realizing asynchronous data access by a host controller in response to an image data transfer request from the host controller, by adding a minimum amount of circuitry to the image output apparatus without using an external data buffer. The image output apparatus includes: a storage device for storing image data; a display circuit for sequentially reading the image data from the storage device and converting the image data into image data capable of being displayed; a timing controller for controlling the operation timing of the display circuit; and an output circuit for changing an operation mode of the timing controller in response to a data transfer request from the host controller and allowing the image data corresponding in amount to the data transfer request to be outputted asynchronously.

Application Filing Date (1):
19980105

Brief Summary Text (5):
Conventional technology in this field will be described with reference to FIG. 2B. A conventional image output apparatus 1 formats image data synchronously with a system clock sclk 5 and horizontal and vertical sync signals of a display device such as a CRT, and outputs the formatted image data. Since the image output apparatus 1 outputs image data of a predetermined format at a predetermined timing, an external data buffer 2 for temporarily storing the image data outputted from the image output apparatus 1 is required if a host controller 4 such as a microprocessor executes a so-called direct memory access (DMA) transfer. Upon reception of a data request host req signal from the microprocessor 4, the image data is asynchronously outputted from an output terminal data out 4' of the data buffer 2.

Detailed Description Text (3):
Although the invention is not limited to this, the RAM interface 7 is adapted to time-divisionally perform an operation of reading image data from the storage device 6 and supplying it to the line buffers 12-1 and 12-2 and an operation of writing image data decoded by the decoder 40 into the storage device 6. The RAM interface 7 has a built-in address counter. When the start address of a desired line is supplied from the timing controller 10 prior to reading the image data, the RAM interface 7 translates this start address into an address for the storage device 6, and automatically reads the image data from the storage device 6 while incrementing the address counter in response to a system clock sclk.

Detailed Description Text (6):
In a usual image output mode, the timing controller 10 controls the digital filter 13 to operate synchronously with a system clock sclk 5 and output image data at a predetermined period via FIFO 14 to the host controller or host CPU 60. The host CPU 60 generates a mode switching signal MDC which switches between a synchronous read mode and an asynchronous read mode. In the synchronous read mode, image data is read at TV signal timings, whereas in the asynchronous mode, image data is read at CPU timings.

Detailed Description Text (7):
Upon reception of the mode switching signal MDC from the host CPU 60, the timing controller 10 stops a supply of the system clock sclk 5 to the digital filter 13, and allows the asynchronous clock generator 15 to supply a non-periodical and

asynchronous clock aclk 17 to the digital filter 13. Starting from this timing, the asynchronous clock generator 15 operates in the asynchronous read mode different from the usual image output mode. In the asynchronous read mode, image data is asynchronously read in response to a data request host req signal 3 supplied from the host CPU 60.

Detailed Description Text (8):
Specifically, if the asynchronous clock generator 15 receives from the host CPU 60 the data request host req signal 3 requesting a transfer of one pixel image data and receives from the timing controller 10 a transfer ready trn rdy signal 26 of the High level indicating a data transfer ready state of the line buffer 12-1, 12-2, then the asynchronous clock generator 15 supplies the asynchronous clock aclk signal 17 synchronizing with the system clock sclk 5 to the digital filter 13 which in turn outputs image data. On the other hand, if the asynchronous clock generator 15 does not receive the one pixel image data transfer request from the host CPU 60 or if the transfer ready tran rdy signal 16 is of a Low level, i.e., if the line buffer 12-1, 12-2 cannot output image data, then the asynchronous clock aclk signal 17 is changed to the Low level to stop outputting image data.

Detailed Description Text (9):
If the line buffer 12-1, 12-2 cannot output image data because of some reason on the side of the image output apparatus, the asynchronous clock generator 15 supplies a host wait host wait signal 20 of the High level to the host CPU 60 to suspend the data transfer request. The timing controller 10 has a function of reading data from and wiring data to the line buffers 12-1 and 12-2. In the asynchronous read mode, the timing controller 10 operates synchronously with the asynchronous clock aclk signal 17 from the asynchronous clock generator 15. If the line buffer 12-1, 12-2 cannot output image data because of some reason on the side of the image output apparatus, the timing controller 10 changes the transfer ready trn rdy signal 16 to the Low level. Although the transfer ready trn rdy signal 16 has the equivalent meaning to the host wait host wait signal 20, these timings are different. Namely, the host wait host wait signal 20 is changed to the Low level after the asynchronous clock generator 15 recognizes the High level of the transfer ready trn rdy signal 16. When the transfer ready trn-rdy signal 16 changes to the Low level, the host wait host wait signal 20 changes to the High level at the same timing.

Detailed Description Text (10):
An embodiment of the timing controller 10 shown in FIG. 1 is detailed in FIG. 3, and its operation timings are illustrated in FIG. 4. The timing controller 10 includes a write address generator 26, a read address generator 25, a controller 27, and a selector 41 for selecting either the system clock sclk or the asynchronous clock aclk in accordance with the mode change MDC signal. The write address generator 26 starts its operation in response to a reset reset signal 30 from the controller 27. In an usual case, image data of one line is written in the line buffer 12-1, 12-2 and a write address Waddr signal 23 is incremented from "0" each time the system clock sclk is supplied. When the write address for the last image data of one line is outputted, a line write end wline end signal 28 is outputted to the controller 27 to thereafter stop the address increment operation. In FIG. 4, one-line write periods are indicated by w0, w1, w2, and w3. The different time durations thereof indicate different amounts of transferred data in one line.

Detailed Description Text (13):
The controller 27 controls the operations of the read and write address generators 25 and 26, synchronously with the system clock sclk signal 5. When the line buffer write period w0 ends and the line write end wline end signal 28 is received from the write address generator 26, the controller 27 outputs the address reset reset signal 30. At this time, since the line buffer 12-1, 12-2 becomes ready for an image data output, the controller 27 changes the data transfer ready trn rdy signal 16 from the Low level to the High level.

Detailed Description Text (15):
The advantages of the embodiment shown in FIG. 3 are as follows. Since the write address generator 26 for controlling data write into the line buffers 12-1 and 12-2 shown in FIG. 1 operates synchronously with the system clock sclk, the transfer time of one line is proportional to the number of transferred pixels and does not depend

on the transfer request from the host CPU 60. Therefore, after the write operation into the line buffer 12-1, 12-2 is completed, the RAM interface 7 can be assigned another task. For example, in the case of a compressed data decoder in conformity with the MPEG video specifications, the RAM interface 7 has many operations other than data transfer to the line buffers 12-1 and 12-2, such as input/output of compressed image data, input/output of reference image data, and input/output of decoded data, and executes these operations time-divisionally. According to the embodiment, unnecessary overhead to be caused by the wait time for a data request from the host CPU 60 can be avoided.

Detailed Description Text (20):
Since FIFO 14 has two buffers (latch circuits), data of one pixel can be outputted after the host wait host wait signal 20 is changed to the High level. If the host CPU 60 reads excessive data from FIFO 14, the relationship between the read control rcnt signal 18 and write control wcnt signal 19 changes. The asynchronous clock controller 32 detects this change in the relationship between the read control rcnt signal 18 and write control wcnt signal 19. If the host CPU 60 reads excessive data and the High level of the transfer ready trn rdy signal 16 is detected while the host wait host wait signal 20 takes the High level, then the asynchronous clock controller 32 inverts the write control wcnt signal 19, loads image data capable of being outputted, into one of the two buffers 39-1 and 39-2 of FIFO 14, and thereafter changes the host wait host wait signal 20 to the Low level to resume the data transfer to the host CPU 60.

Detailed Description Text (21):
FIG. 7 shows operation timings of the embodiment circuits shown in FIGS. 5 and 6. Each time the write control wcnt signal 19 changes, 0th, 2nd, and 4th image data are written in the latch circuit 39-1, and 1st, 3rd, and 5th image data are written in the latch circuit 39-2. Each time the read control rcnt signal 18 changes, image data in the latch circuits 39-1 and 39-2 are alternately read. As a result, the image data is read from FIFO 14 in the order of 0th, 1st, 2nd, 3rd, and 4th. In this manner, asynchronous transfer to the host CPU 60 can be realized by a simple control circuit only by providing two FIFOs at the output stage.

First Hit Fwd Refs

Generate Collection Print

L4: Entry 1 of 11 File: USPT Aug 19, 2003

DOCUMENT-IDENTIFIER: US 6608647 B1
TITLE: Methods and apparatus for charge coupled device image acquisition with independent integration and readout

Application Filing Date (1):
19980529

Brief Summary Text (20):
Still further aspects of the invention provide an image acquisition apparatus as described above in which multiple head units are provided, each associated with a respective CCD. The control unit of such can apparatus can effect synchronous image acquisition from those head units by applying shutter pulses substantially concurrently to them. Alternatively, the images can be acquired asynchronously via application of shutter pulses at different times. Whether image acquisition is synchronous or asynchronous, the control unit can control image transfer from the head units by applying readout signals to them independently of the application of the shutter pulses. Thus, for example, in response to requests from the host, the control unit can cause images acquired simultaneously by multiple head units to be output to the host memory in any desired order.

First Hit Fwd Refs

Generate Collection Print

L4: Entry 2 of 11 File: USPT Mar 12, 2002

DOCUMENT-IDENTIFIER: US 6356314 B1
TITLE: Image synthesizing device and image conversion device for synthesizing and displaying an NTSC or other interlaced image in any region of a VCA or other non-interlaced image

Application Filing Date (1):
19990909

Brief Summary Text (34):
The ninth invention is an image conversion device which converts interlaced scan image signals composed of odd-numbered fields and even-numbered fields into non-interlaced scan image signals, comprising: one serial access memory with which write and read operations can be performed asynchronously and which sequentially stores interlaced scan image signals in an address region incremented synchronously with inputted clock signals; write clock formation means for extracting control-use synchronization signals from inputted interlaced scan image signals and forming write-use clock signals with respect to the serial access memory on the basis of the extracted signals; high-speed clock signal generation means for generating high-speed clock signals with a higher frequency than the write-use clock signals; first write control means for storing image data of one of the fields in an intermittent address region of the serial access memory corresponding to an order of lines in the one field by alternately executing a first operation, in which one line of interlaced scan image data is written while the write address of the serial access memory is incremented synchronously with the write-use clock signals when image data of one of the fields of the interlaced scan image signals has been inputted, and a second operation, in which the write address of the serial access memory is incremented by an amount equal to the address region corresponding to one line of image data synchronously with the high-speed clock signals without data writing being performed, with a leading address of the serial access memory serving as an origin; second write control means for storing, corresponding to an order of lines in the other field, image data of the other field in empty address regions formed between the address regions where the image of the lines of the one field of the serial access memory is stored by alternately executing a third operation, in which one line of interlaced scan image data is written while the write address of the serial access memory is incremented synchronously with the write-use clock signals when image data of the other field of the interlaced scan image signals has been inputted, and a fourth operation, in which the write address of the serial access memory is incremented by an amount equal to the address region corresponding to one line of image data synchronously with the high-speed clock signals without data writing being performed, with an address advanced by an address region corresponding to one line of image data from the leading address serving as the origin; and read control means for reading, in the address order from the leading address, the interlaced scan image data stored in the serial access memory by the first and second write control means; and wherein interlaced signals are converted into non-interlaced signals through the one serial access memory.

Brief Summary Text (36):
The tenth invention is an image synthesizing device with which a sub-image included in a specific extraction region of an interlaced scan sub-image composed of odd-numbered fields and even-numbered fields is synthesized and displayed within a

specific display region on a display screen on which a non-interlaced scan main image is displayed, comprising: one serial access memory with which write and read operations can be performed asynchronously and which sequentially stores sub-image signals in an address region which is advanced synchronously with inputted clock signals; write clock formation means for extracting control-use synchronization signals from inputted sub-image signals and forming write-use clock signals with respect to the serial access memory on the basis of the extracted signals; high-speed clock signal generation means for generating high-speed clock signals with a higher frequency than the write-use clock signals; first write control means for storing the image data to be displayed in the display region of one of the fields out of the sub-image signals in an intermittent address region of the serial access memory corresponding to an order of lines in the one field by alternately executing a first operation, in which one line of data to be displayed in the display region of the one field is written while the write address of the serial access memory is incremented synchronously with the write-use clock signals when an image of the one field has been inputted and when the sub-image included in the specific extraction region has been inputted, and a second operation, in which the write address of the serial access memory is incremented by an amount equal to the address region corresponding to one line of sub-image data to be displayed in the display region synchronously with the high-speed clock signals without data writing being performed, with a leading address of the serial access memory serving as an origin; second write control means for storing, corresponding to an order of lines in the other field out of the sub-image signals, the image data to be displayed in the display region of the other field in empty address regions formed between the address regions where the image of the lines of the one field of the serial access memory is stored by alternately executing a third operation, in which one line of data to be displayed in the display region of the other field is written while the write address of the serial access memory is incremented synchronously with the write-use clock signals when an image of the other field has been inputted and when the sub-image included in the specific extraction region has been inputted, and a fourth operation, in which the write address of the serial access memory is incremented by an amount equal to the address region corresponding to one line of sub-image data to be displayed in the display region synchronously with the high-speed clock signals without data writing being performed, with an origin address being an address advanced from the leading address by an amount equal to the address region corresponding to one line of image data to be displayed in the display region; read control means for reading, in the address order from the leading address, the sub-image data stored in the serial access memory by the first and second write control means when the scanning address of the main image is an address corresponding to the specific display region; and switching means for selecting the main image when the scanning address of the main image is not an address corresponding to the specific display region, and selecting and outputting the sub-image outputted from the serial access memory when the scanning address of the main image is an address corresponding to the specific display region.

CLAIMS:

5. An image conversion device which converts interlaced scan image signals composed of odd-numbered fields and even-numbered fields into non-interlaced scan image signals, comprising:

one serial access memory with which write and read operations can be performed asynchronously and which sequentially stores interlaced scan image signals in an address region incremented synchronously with inputted clock signals;

write clock formation means for extracting control-use synchronization signals from inputted interlaced scan image signals and forming write-use clock signals with respect to the serial access memory on the basis of the extracted signals;

high-speed clock signal generation means for generating high-speed clock signals

h e b b cg b cc e

with a higher frequency than the write-use clock signals;

first write control means for storing the image data of one of the fields in an intermittent address region of the serial access memory corresponding to an order of lines in the one field by alternately executing a first operation, in which one line of interlaced scan image data is written while the write address of the serial access memory is incremented synchronously with the write-use clock signals when image data of one of the fields of the interlaced scan image signals has been inputted, and a second operation, in which the write address of the serial access memory is incremented by an amount equal to the address region corresponding to one line of image data synchronously with the high-speed clock signals without data writing being performed, with a specific address of the serial access memory serving as a first origin address;

second write control means for storing, corresponding to an order of lines in the other field, image data of the other field in empty address regions formed between the address regions where the image of the lines of the one field of the serial access memory is stored by alternately executing a third operation, in which one line of interlaced scan image data is written while the write address of the serial access memory is incremented synchronously with the write-use clock signals when image data of the other field of the interlaced scan image signals has been inputted, and a fourth operation, in which the write address of the serial access memory is incremented by an amount equal to the address region corresponding to one line of image data synchronously with the high-speed clock signals without data writing being performed, with a second origin address advanced by an address region corresponding to one line of image data from the first origin address serving as the origin; and

read control means for reading, in the address order from the first origin address, the interlaced scan image data stored in the serial access memory by the first and second write control means;

and wherein one frame of interlaced scan image signals are packed and stored in a continuous address region of the serial access memory.

6. An image synthesizing device with which a sub-image included in a specific extraction region of an interlaced scan sub-image composed of odd-numbered fields and even-numbered fields is synthesized and displayed within a specific display region on a display screen on which a non-interlaced scan main image is displayed, comprising:

one serial access memory with which write and read operations can be performed asynchronously and which sequentially stores sub-image signals in an address region which is advanced synchronously with inputted clock signals;

write clock formation means for extracting control-use synchronization signals from inputted sub-image signals and forming write-use clock signals with respect to the serial access memory on the basis of the extracted signals;

high-speed clock signal generation means for generating high-speed clock signals with a higher frequency than the write-use clock signals;

first write control means for storing the image data to be displayed in the display region of one of the fields out of the sub-image signals in an intermittent address region of the serial access memory corresponding to an order of lines in the one field by alternately executing a first operation, in which one line of data to be displayed in the display region of the one field is written while the write address of the serial access memory is incremented synchronously with the write-use clock signals when an image of the one field has been inputted and when the sub-image included in the specific extraction region has been inputted, and a second

operation, in which the write address of the serial access memory is incremented by an amount equal to the address region corresponding to one line of sub-image data to be displayed in the display region synchronously with the high-speed clock signals without data writing being performed, with a specific address of the serial access memory serving as a first origin address;

second write control means for storing, corresponding to an order of lines in the other field out of the sub-image signals, the image data to be displayed in the display region of the other field in empty address regions formed between the address regions where the image of the lines of the one field of the serial access memory is stored by alternately executing a third operation, in which one line of data to be displayed in the display region of the other field is written while the write address of the serial access memory is incremented synchronously with the write-use clock signals when an image of the other field has been inputted and when the sub-image included in the specific extraction region has been inputted, and a fourth operation, in which the write address of the serial access memory is incremented by an amount equal to the address region corresponding to one line of sub-image data to be displayed in the display region synchronously with the high-speed clock signals without data writing being performed, with an origin address being a second origin address advanced from the first origin address by an amount equal to the address region corresponding to one line of image data to be displayed in the display region;

read control means for reading, in the address order from the first origin address, the sub-image data stored in the serial access memory by the first and second write control means when the scanning address of the main image is an address corresponding to the specific display region; and

switching means for selecting the main image when the scanning address of the main image is not an address corresponding to the specific display region, and selecting and outputting the sub-image outputted from the serial access memory when the scanning address of the main image is an address corresponding to the specific display region;

and wherein one frame of interlaced scan image signals are packed and stored in a continuous address region of the serial access memory.

L4: Entry 5 of 11 File: USPT Jan 2, 1990

DOCUMENT-IDENTIFIER: US 4891768 A
TITLE: Raster image processor

Abstract Text (1):
Raster image processor for filling a page-size raster image memory and for the conversion of the data stored in the raster image memory into a serial pixel-bit stream for a raster output scanner which includes a microprogrammable central processing unit; a raster image bus interface connected to a synchronous raster image bus system; a raster output scanner interface connected to the raster output scanner; an interface connected to the asynchronous bus system; and a synchronous raster image processor bus system connecting the microprogrammable CPU to the raster image bus interface to the raster output scanner interface, and to the interface which is connected to the asynchronous bus system.

Application Filing Date (1):
19860926

First Hit

Generate Collection Print

L4: Entry 7 of 11 File: JPAB Sep 29, 2000

PUB-NO: JP02000270259A
DOCUMENT-IDENTIFIER: JP 2000270259 A
TITLE: TS SIGNAL FADE CONTROLLER AND METHOD FOR CONTROLLING TS SIGNAL FADE

PUBN-DATE: September 29, 2000

INVENTOR-INFORMATION:
NAME COUNTRY
WATANABE, CHIAKI

ASSIGNEE-INFORMATION:
NAME COUNTRY
NEC CORP

APPL-NO: JP11067206
APPL-DATE: March 12, 1999

INT-CL (IPC): H04 N 5/262; H04 N 7/32

ABSTRACT:

PROBLEM TO BE SOLVED: To attain fade-out and fade-in of a picture.

SOLUTION: The controller is provided with a picture type identification section 101 that detects a picture header from a received TS signal and provides an output of a picture type and an incidence timing signal of the picture type, an I picture storage section 102 that stores coded data in an I picture mode, a P picture storage section 103 that stores coded data in a P picture mode, and a B picture storage section 104 that stores coded data in a B picture mode, a changeover section 105 that selects coded data and outputs the selected data, an image synchronization signal generating section 106 that outputs a signal resulting from synchronizing a fade control signal received asynchronously with picture data including a received Ts signal, and a changeover device 107 that changes over the received Ts signal or the signal from a changeover section with a signal outputted from the image synchronization signal generating section 106.

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 1 of 1 returned.

☐ 1. Document ID: JP 04170857 A

L6: Entry 1 of 1 File: JPAB Jun 18, 1992

PUB-NO: JP404170857A
DOCUMENT-IDENTIFIER: JP 04170857 A
TITLE: PICTURE DATA MEMORY DEVICE

PUBN-DATE: June 18, 1992

INVENTOR-INFORMATION:

NAME	COUNTRY
YAMAZAKI, SHUICHI	

ASSIGNEE-INFORMATION:

NAME	COUNTRY
RICOH CO LTD	

APPL-NO: JP02299436
APPL-DATE: November 5, 1990

INT-CL (IPC): H04N 1/21; B41J 5/30; G03G 15/04

ABSTRACT:

PURPOSE: To use only the memories of two systems by providing a write means which alternately writes picture data in first and second FIFO memories in a prescribed period and read control means which start the reading at speed more than picture data write speed in asynchronizing with the write means.

CONSTITUTION: The write means CLK, LSYNC 102 which alternately writes picture data in the first and second FIFO memories 100 and 101 in the prescribed period is provided. Then, the read control means DEPT, RCLK 103-105 which start the reading at speed more than the picture data write speed of the write means CLK, LSYNC 102 of the FIFO memory which the write means CLK, LSYNC 102 does not select for writing at the period equal to the prescribed period in asynchronizing with the write means CLK, LSYNC 102 are provided. Thus, only the memories of two systems are required.

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

h e b b cg b e e ch e c f

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
JP-04170857-A.did.	1

Display Format: TI Change Format

Previous Page Next Page Go to Doc#

h e b b cg b e e ch e c f

First Hit

Generate Collection Print

L4: Entry 10 of 11 File: DWPI Jun 18, 1992

DERWENT-ACC-NO: 1992-254219
DERWENT-WEEK: 199954

TITLE: Image data buffer memory for image processor - transfers synchronously with scanning of printer image data read by scanner to printer recording asynchronously with scanner NoAbstract

PATENT-ASSIGNEE:

ASSIGNEE	CODE
RICOH KK	RICO

PRIORITY-DATA: 1990JP-0299436 (November 5, 1990)

Search Selected Search ALL Clear

PATENT-FAMILY:

	PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
☐	JP 04170857 A	June 18, 1992		007	H04N001/21
☐	JP 2978232 B2	November 15, 1999		006	H04N001/21

APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-NO	DESCRIPTOR
JP 04170857A	November 5, 1990	1990JP-0299436	
JP 2978232B2	November 5, 1990	1990JP-0299436	
JP 2978232B2		JP 4170857	Previous Publ.

INT-CL (IPC): B41J 5/30; G03G 15/04; H04N 1/21
ABSTRACTED-PUB-NO: JP 04170857A
EQUIVALENT-ABSTRACTS:

CHOSEN-DRAWING: Dwg.1/2

TITLE-TERMS: IMAGE DATA BUFFER MEMORY IMAGE PROCESSOR TRANSFER SYNCHRONOUS SCAN PRINT IMAGE DATA READ SCAN PRINT RECORD ASYNCHRONOUS SCAN NOABSTRACT

ADDL-INDEXING-TERMS:
FIFO

DERWENT-CLASS: P75 P84 S06 T04 W02

EPI-CODES: S06-A03; T04-G10; W02-J03D;

SECONDARY-ACC-NO:

h e b b cg b cc e

Non-CPI Secondary Accession Numbers: N1992-193951

h e b b cg b cc e